increases in performance. This follows from the fact that the dominant time constant is defined by the gate output resistance and parasitic and input capacitance; the additional resistance from a metal line does not significantly increase the delay. Superconducting lines could theoretically be designed on a much finer pitch than metal lines, reducing parasitic capacitance and line length. Unfortunately, superconductors exacerbate the ringing problem caused by impedance mismatch. Much development remains before high-temperature, thin-film superconductors can be patterned into fine lines and integrated into a semiconductor process. The increased cost of using any new technique must be weighed against anticipated gains in performance. For superconductors, the reduction in intrachip interconnect delay is small compared to that of air-bridge interconnects.

The most realistic and cost-effective approaches to improving interconnect delays are further development of air-bridge interconnect systems, and development of design methodologies and computer-aided design tools for minimizing interconnect length.

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An Enhanced Technique for Simulating Short-Circuit Power Dissipation

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***Abstract*—A circuit simulation technique which permits the measurement of the average short-circuit power dissipation component in integrated circuits using SPICE is presented. It is an extension of a previously presented scheme [1] which measures average power dissipation while circuits are being simulated. This extended technique is most appropriate for low-power circuit design. It can be applied effectively to any complementary circuit structure, such as CMOS, that does not permit current flow (other than leakage current) during steady-state operation. Results for differently ratioed *Wp/Wn* CMOS circuits are shown.**

I. INTRODUCTION

The goal of this correspondence is to present a technique that accurately measures the average short-circuit (i.e., crossover) current in complementary circuit structures where no current can flow (other than leakage current) during steady-state operation since no dc path between power and ground exists. The emphasis is on the concept of current component isolation as a means for determining the magnitude of the short-circuit power dissipation component. There has been no direct treatment in the literature of short-circuit power dissipation simulation techniques. However, a very useful contribution by Kang [1] describes a method for accurately and conveniently simulating average power dissipation using a single power meter consisting of a single dependent current source in parallel with an *RC* circuit. Fisher [2] elegantly enhances Kang's power meter by adding a nonlinear dependent current source to improve the versatility and accuracy at the expense of adding a control signal. A thorough discussion and analysis of short-circuit power dissipation in static CMOS circuitry with specific application to the optimal design of cascaded buffers are also found in [3].

The technique described within this correspondence utilizes power meters similar to those of Kang's, placed appropriately in pairs, to measure short-circuit power dissipation. The specific power meters used here serve to illustrate the current component isolation concept and can be replaced by other types of power meters for measuring current.

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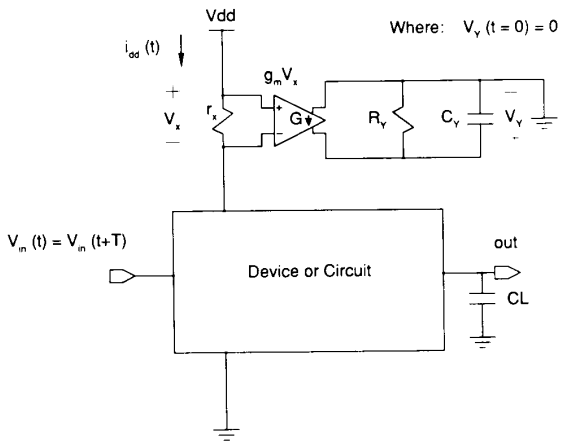

Fig. 1. A circuit connected to a voltage-controlled current source and a parallel *RC* circuit for measuring the average power consumption by directly reading $V_Y(T)$.

II. AVERAGE SHORT-CIRCUIT POWER DISSIPATION MEASUREMENT

A. Derivation of Average Power Dissipation

The scheme used in [1] to simulate average power dissipation is shown in Fig. 1. The power meter circuitry consists of a voltage-controlled current source shunted with a parallel *RC* circuit. The average power is read as the voltage V_Y across the initially uncharged capacitor C_Y at time T for a correctly chosen gain g_m. The series resistance r_x must be small enough to cause no disturbances in $i_{dd}(t)$. The derivation from [1] gives the voltage $V_Y(T)$ as

$$V_Y(T) = g_m \frac{r_x}{C_Y} \int_0^T e^{\alpha(t-\tau)} i_{dd}(\tau)\, d\tau$$

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where

$$a = \frac{1}{R_Y C_Y}$$

$$V_Y(0) = 0.$$

If R_Y and C_Y are chosen such that

$$R_Y C_Y \gg T$$

over the region of interest for which T is considered, then $V_Y(T)$ can be approximated by

$$V_Y(T) = g_m \frac{r_x}{C_Y} \int_0^T i_{dd}(\tau)\, d\tau.$$

The average power dissipation of the circuit is given by

$$P_{\text{ave}} = \left(\frac{V_{dd}}{T}\right) \int_0^T i_{dd}(\tau)\, d\tau.$$

If a value for g_m is chosen such that

$$g_m = \frac{V_{dd}}{T} \frac{C_Y}{r_x}$$

then

$$V_Y(T) = P_{\text{ave}}.$$

B. Measurement of Average Short-Circuit Power Dissipation

The scheme described in subsection A above is extended to permit measurement of the average short-circuit power dissipation. A power meter pair is needed to measure the short-circuit power component of static circuits whose signal outputs transition and settle to the same voltage level. This is depicted in Fig. 2, where P_1, P_2, P_3, and P_4 are the power meters.

P_1 and P_2 is the first power meter pair which measures the average power dissipation of the odd stages of the circuitry whose outputs transition and settle to the same voltage level. Assuming that these outputs transition and settle from a high voltage level at $t = 0$ to a low one at $t = t_1$ and back to a high at $t = T$, then the average short-circuit power dissipation component $P_{SC0}(T)$ is given by

$$P_{SC0}(T) = P_1(T) - P_2(t_1) + P_1(t_1).$$

Similarly, P_3 and P_4 make up the second power meter pair, which measures the average power dissipation of the even stages of the circuitry whose outputs transition and settle to the inverse voltage state as those of the odd stages. In this case the average short-circuit power dissipation component P_{SCE} at $t = T$ is given by

$$P_{SCE}(T) = P_3(T) - P_3(t_1) + P_4(t_1).$$

Thus, the total average short-circuit power dissipation $P_{SC}(T)$ is given by

$$P_{SC}(T) = P_{SC0}(T) + P_{SCE}(T).$$

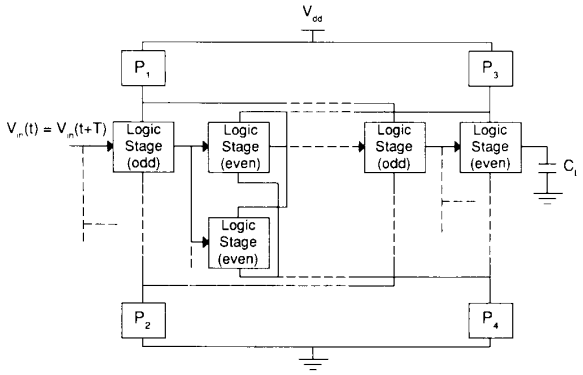


Fig. 2. A circuit setup which permits simulation of average short-circuit power consumption by utilizing the power meter pair concept. The power meter pairs are P_1, P_2 and P_3, P_4.

III. Application to CMOS Circuitry

We have selected a relatively complex circuit to illustrate the extended technique described above. Fig. 3 represents a circuit consisting of two sections, each running at a different signal rate $1/T$, and each possessing two power meter pairs. SPICE2G.6 simulations were run at a temperature of 27°C and a power supply equal to 5 V. As in [1], we selected $R_Y = 10^{12}\ \Omega$, $C_Y = 1$ pF, and $r_x = 10^{-6}\ \Omega$ for each of the four power meters. The signal period for block A was chosen to be $T = 100$ ns and therefore $g_{m1} = 50$ mho while block B was $T = 200$ ns with $g_{m2} = 25$ mho. The SPICE simulation results are shown in Fig. 4. The average short-circuit power dissipation $P_{SC\,A}(T)$ for block A is shown in Fig. 4(a) and computed as follows:

$$P_{SC\,A}(T) = P_{SC0}(T) + P_{SCE}(T)$$
$$P_{SC\,A}(T) = \{P_1(T) - P_2(t_1) + P_1(t_1)\} + \{P_3(T) - P_3(t_1) + P_4(t_1)\}$$
$$P_{SC\,A}(T) = \{3.1\text{ mW} - 2.7\text{ mW} + 0.4\text{ mW}\} + \{2.9\text{ mW} - 2.1\text{ mW} + 0.6\text{ mW}\}$$
$$P_{SC\,A}(T) = 2.2\text{ mW}.$$

Similarly, the average short-circuit power dissipation $P_{SC\,B}(T)$ for block B is shown in Fig. 4(b) and is computed as follows:

$$P_{SC\,A}(T) = P_{SC0}(T) + P_{SCE}(T)$$
$$P_{SC\,B}(T) = \{P_6(T) - P_6(t_1) + P_5(t_1)\} + \{P_7(T) - P_7(t_1) + P_8(t_1)\}$$
$$P_{SC\,B}(T) = \{3.3\text{ mW} - 2.4\text{ mW} + 0.3\text{ mW}\} + \{3.8\text{ mW} - 3.1\text{ mW} + 0.3\text{ mW}\}$$
$$P_{SC\,B}(T) = 2.2\text{ mW}.$$

Thus, the total average short-circuit power dissipation of the circuit in Fig. 3 is

$$P_{SC}(T) = P_{SC\,A}(T) + P_{SC\,B}(T) = 4.4\text{ mW}.$$

The above simulations were carried out for a transistor device ratio of $Wp/Wn = 1$. In the case of NAND and NOR gates, Wp and Wn were computed as an effective parallel or series combina-

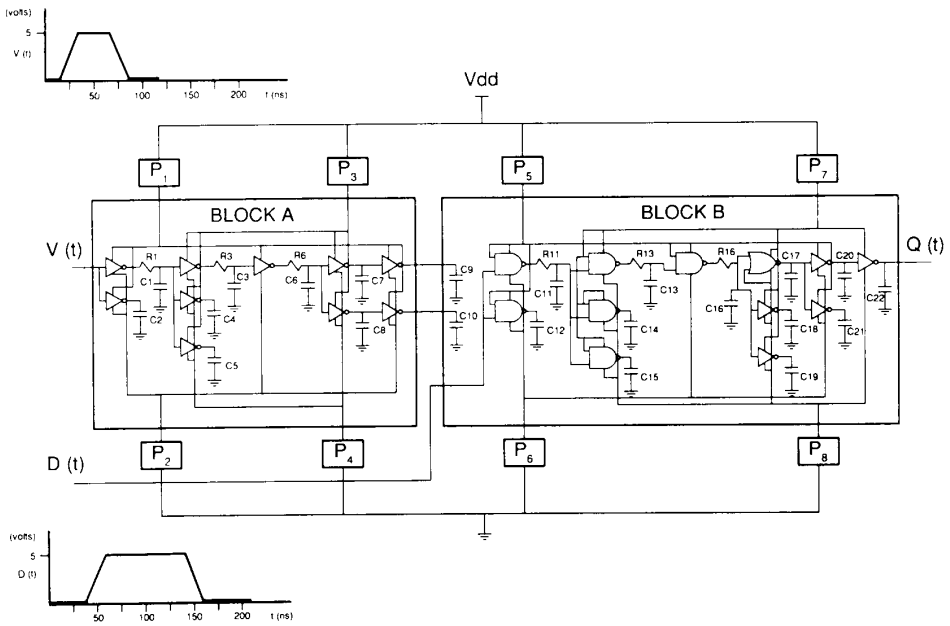
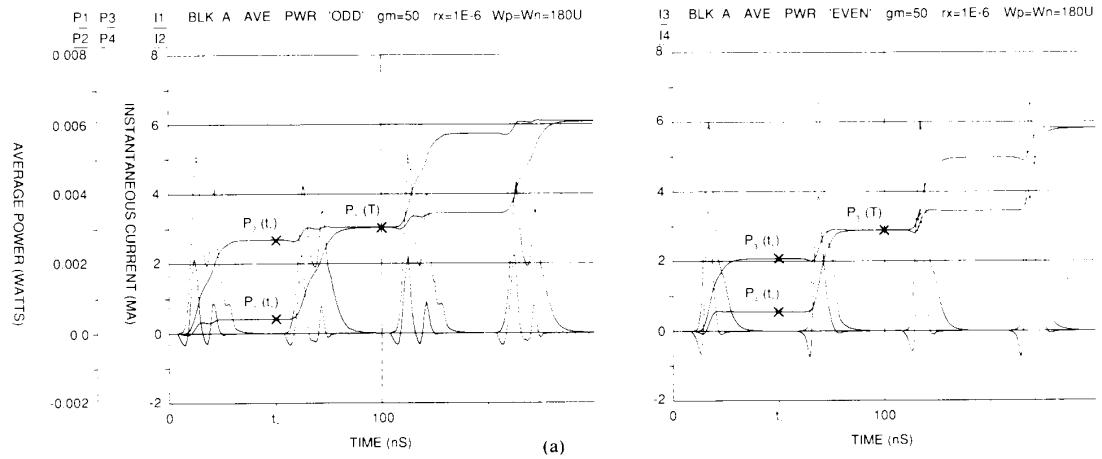


Fig. 3. A CMOS circuit, consisting of two sections, used to simulate average short-circuit power consumption. The setup of each section follows the convention described in Section II-B and illustrated in Fig. 2. The combinational readings of the power meter pairs conveniently supply the average short-circuit power dissipated during circuit simulation.



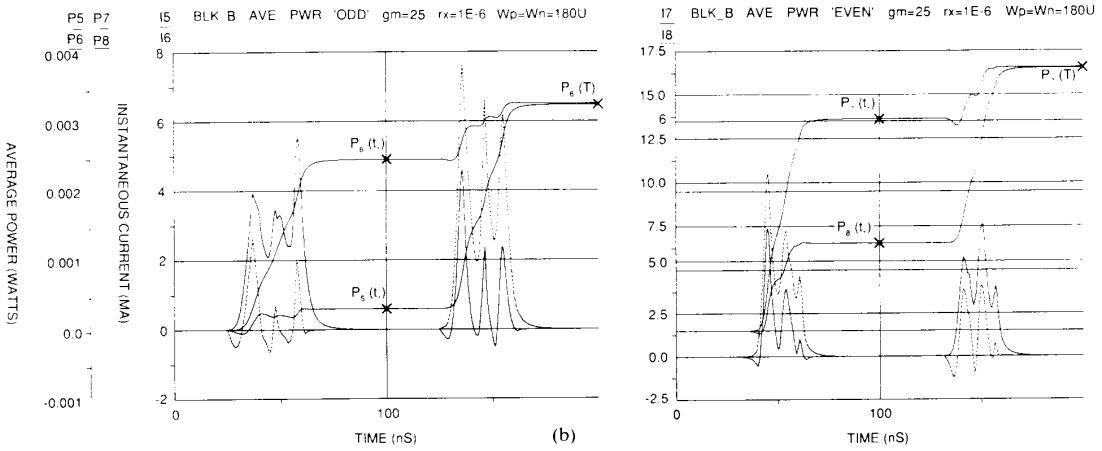


Fig. 4. Average short-circuit power consumption SPICE curves for the circuit in Fig. 3. The curves in (a) characterize block *A* and the curves in (b) characterize block *B*.

TABLE I
POWER DISSIPATION COMPONENT MEASUREMENTS FOR FIG. 3 AS Wp/Wn VARIES WITH FIXED LOAD, INPUT TRANSITION TIMES, AND SIGNAL PERIOD T

Wp/Wn Ratio	Pave	Psc	Pd	Psc/Pd
	(mW)	(mW)	(mW)	
2/3	16.02	5.93	10.09	0.59
1	13.1	4.4	8.7	0.50
3/2	9.35	2.95	6.3	0.47
2	8.7	2.7	6.0	0.45

tion. The circuit in Fig. 3 was simulated for different Wp/Wn ratios and the results are tabulated in Table I. The term P_d, average dynamic power, in column 4 was computed as the difference between $P_{ave}(T)$ and $P_{SC}(T)$. Column 5 depicts the power efficiency P_{SC}/P_d.

IV. CONCLUSION

An extension to a previously presented scheme [1] for measuring average power dissipation in complementary integrated circuits is presented. The extended technique is applicable to circuits which have no current flow during a circuit's steady-state operation other than leakage current. The scheme requires a SPICE circuit configuration in which the voltage output state of each cascaded logic stage inverts the incoming voltage state. This extended technique utilizes power meter pairs to isolate the average short-circuit current from the total average current, thereby providing the average short-circuit power dissipation. The proposed technique was effectively applied to a variety of differently ratioed Wp/Wn CMOS circuits. This technique for simulating the average short-circuit power dissipation is most applicable in the design of low-power customized circuits and for characterizing the power efficiency of standard cell libraries.

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Erratum to "Fully Differential Operational Amplifiers with Accurate Output Balancing"

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In the above paper[1], the vertical axes of Fig. 2(a) and Fig. 4(a) should be interchanged.

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