AN ACCURATE SIMULATION TECHNIQUE FOR SHORT-CIRCUIT POWER DISSIPATION BASED ON CURRENT COMPONENT ISOLATION

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Abstract

This paper describes a circuit simulation technique which permits the measurement of the average short-circuit power dissipation component in integrated circuits. This technique is most appropriate for low power circuit design and can be applied effectively to any complementary circuit structure, such as CMOS, that does not permit current flow (other than leakage current) during steady state operation. Short-circuit power dissipation expressions are derived and SPICE simulation results for a differently ratioed W_p/W_n circuit are shown.

I. Introduction

The goal of this paper is to present a technique that accurately measures the average short-circuit current in complementary circuit structures, where no current can flow (other than leakage current), during steady state operation since no DC path between power and ground exists. Emphasis is on the concept of current component isolation as a means for determining the magnitude of the short-circuit power dissipation component. Kang [1] describes a method for accurately and conveniently simulating average power dissipation using a single power meter consisting of a single dependent current source in parallel with an RC circuit. Fisher [2] elegantly enhances Kang's power meter by adding a nonlinear dependent current source to improve the versatility and accuracy at the expense of adding a control signal. A thorough discussion and analysis of short-circuit power dissipation in static CMOS circuitry with specific application to the optimal design of cascaded buffers is also found in [3].

The technique described within this paper utilizes power meters similar to those of Kang's, placed appropriately in pairs, to measure short-circuit power dissipation. The specific power meters used here serve to illustrate the current component isolation concept and can be replaced by other power meter types for measuring current.

II. List of Symbols

f	=	frequency (1/T)
g_m	=	transfer conductance of voltage controlled current source
$i_{sc}(t)$	=	instantaneous short-circuit current
$i_d(t)$	=	instantaneous dynamic current
$i_{dd}(t)$	=	total instantaneous current $(i_{sc}(t) + i_d(t))$
$(P_{sc})^{HL}$	=	short-circuit power dissipation for output high to low transition; $((V_{dd}/T)\int_0^{\tau_f} i_{sc}(\tau)\,d\tau)$
$(P_{sc})^{LH}$	=	short-circuit power dissipation for output low to high transition; $((V_{dd}/T)\int_0^{\tau_r} i_{sc}(\tau)\,d\tau)$
$(P_d)^{HL}$	=	dynamic power dissipation for output high to low transition; $((C/T)\int_0^{Vdd} V_{out}dV_{out})$
$(P_d)^{LH}$	=	dynamic power dissipation for output low to high transition; $((C/T)\int_0^{Vdd} V_{out}dV_{out})$
P_{sc}	=	total short-circuit power dissipation $((P_{sc})^{HL} + (P_{sc})^{LH})$
P_d	=	total dynamic power dissipation $((P_d)^{HL} + (P_d)^{LH})$
P_{ave}	=	total average power dissipation $(P_{sc} + P_d)$
T	=	time-period of a signal
t	=	time
τ_r, τ_f	=	input or output rise and fall times of a signal
V_{tp}, V_{tn}	=	threshold voltages of PMOS and NMOS transistors respectively
V_{dd}	=	power supply voltage
W_p	=	channel width of PMOS transistor
W_n	=	channel width of NMOS transistor

III. Average Short-Circuit Power Dissipation

(a) Derivation of Average Power Dissipation

The scheme used in [1] to simulate average power dissipation is shown in Figure 1. The power meter circuitry consists of a voltage-controlled current source shunted with a parallel RC circuit. The average power is read as the voltage V_Y across the initially uncharged capacitor C_Y at time T for a correctly chosen

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gain g_m. The series resistance r_x must be small enough to cause no disturbances in $i_{dd}(t)$. The derivation from [1] gives the voltage $V_Y(T)$ as

$$V_Y(T) = g_m \frac{r_x}{C_Y} \int_0^T e^{-a(t-\tau)}\, i_{dd}(\tau)\, d\tau$$

where

$$a = \frac{1}{R_Y C_Y},\ V_Y(0) = 0$$

If R_Y and C_Y are chosen such that

$$R_Y C_Y >> T$$

over the region of interest for which T is considered then $V_Y(T)$ can be approximated by

$$V_Y(T) = g_m \frac{r_x}{C_Y} \int_0^T i_{dd}(\tau)\, d\tau \tag{1}$$

The average power dissipation of the circuit is given by

$$P_{ave} = \left[\frac{V_{dd}}{T}\right] \int_0^T i_{dd}(\tau)\, d\tau$$

If a value for g_m is chosen such that

$$g_m = \frac{V_{dd}}{T} \frac{C_x}{r_x} \tag{2}$$

then

$$V_Y(T) = P_{ave}$$

(b) Derivation of Average Short-Circuit Power Dissipation

Basic Inverting Buffer Case

The scheme described in part (a) above is extended to permit measurement of the average short-circuit power dissipation. A power meter pair is needed to measure the short-circuit power component of static circuits whose signal outputs transition and settle to the same voltage level. Assume an input signal with arbitrarily asymmetric rise and fall times $V_{in}(t) = V_{in}(t+T)$ and an inverting buffer cell between a power meter pair P_1, P_2 as depicted in Figure 2. This will cause unequal short-circuit power dissipations for $(P_{sc})^{LH}$ and $(P_{sc})^{HL}$. If the output transitions and settles from a high voltage level at $t = 0$ to a low at $t = t_1$ and back to a high at $t = T$, then the average short-circuit power dissipation expressions for the top meter can be written as

$$P_1(t_1) = (P_{sc})^{HL} \quad \text{given} \quad P_1(t=0) = 0 \tag{3}$$

$$P_1(T) = (P_{sc})^{HL} + (P_d)^{LH} + (P_{sc})^{LH} \tag{4}$$

Effectively, the short-circuit current component will disappear when the input rise time τ_r reaches $V_{dd} - V_{tp}$, but without any loss of generality, the value of $P_1(t_1)$ is measured when it reaches steady state (i.e., when current flow disappears at time t_1). Similarly, the short-circuit current will effectively disappear when the input fall time τ_f reaches V_{tn}, but again the value of $P_1(T)$ is measured when it reaches steady state. The average short-circuit power dissipation expressions for the bottom meter can be written as

$$P_2(t_1) = (P_{sc})^{HL} + (P_d)^{HL} \tag{5}$$

$$P_2(T) = (P_{sc})^{HL} + (P_d)^{HL} + (P_{sc})^{LH} \tag{6}$$

Finally, the total average short-circuit power dissipation can be deduced by subtracting equation (5) from equation (6) and adding the result to equation (3) thus yielding

$$P_{sc}(T) = P_2(T) - P_2(t_1) + P_1(t_1) \tag{7}$$

General Case

The above scheme can be further extended to permit measurement of the average short-circuit power dissipation of general circuit set-ups. This is depicted in Figure 3, where P_1, P_2, P_3, and P_4 are the power meters. P_1 and P_2 is the first power meter pair which measures the average power dissipation of the odd stages of the circuitry whose outputs transition and settle to the same voltage level. Assuming that these outputs transition and settle from a high voltage level at $t = 0$ to a low at $t = t_1$ and back to a high at $t = T$, then the average short circuit power dissipation component $P_{SCO}(T)$ is given by

$$P_{SCO}(T) = P_2(T) - P_2(t_1) + P_1(t_1) \tag{8}$$

Similarly, P_3 and P_4 is the second power meter pair which measures the average power dissipation of the even stages of the circuitry whose outputs transition and settle to the inverse voltage state as those of the odd stages. In this case the average short circuit power dissipation component P_{SC2} at $t = T$ is given by

$$P_{SCE}(T) = P_3(T) - P_3(t_1) + P_4(t_1) \tag{9}$$

Thus, the total average short-circuit power dissipation $P_{SC}(T)$ is given by

$$P_{SC}(T) = P_{SCO}(T) + P_{SCE}(T) \tag{10}$$

IV. Application to CMOS Circuitry

Figure 4 represents a circuit consisting of two sections, each running at a different signal rate $1/T$, and each possessing two power meter pairs. SPICE2G.6 simulations were run at a temperature of 27°C and power supply equal to 5V. As in [1], we selected $R_Y = 10^{12}\Omega$, $C_Y = 1$ pF and $r_x = 10^{-6}\Omega$ for each of the four power meters. The signal period for block A was chosen to be $T = 100$ns and therefore $g_{m1} = 50$ Mho while block B was $T = 200$ns with $g_{m2} = 25$ Mho. The SPICE simulation results are shown in Figure 5. The average short-circuit power dissipation $P_{SCA}(T)$ for block A is shown in Figure 5a and using equation (10) is computed as follows:

$$P_{SCA}(T) = \quad P_{SCO}(T) \quad + \quad P_{SCE}(T)$$

$$P_{SCA}(T) = \{P_2(T) - P_2(t_1) + P_1(t_1)\} + \{P_3(T) - P_3(t_1) + P_4(t_1)\}$$

$$P_{SCA}(T) = \{3.1mW - 2.7mW + 0.4mW\} + \{2.9mW + 0.6mW\}$$

$$P_{SCA}(T) = 2.2mW$$

Similarly, the average short-circuit power dissipation $P_{SCB}(T)$ for block B is shown in Figure 5b and using equation (10) is computed as follows:

$$P_{SCA}(T) = \quad P_{SCO}(T) \quad + \quad P_{SCE}(T)$$

$$P_{SCB}(T) = \{P_6(T) - P_6(t_1) + P_5(t_1)\} + \{P_7(T) - P_7(t_1) + P_8(t_1)\}$$

$$P_{SCB}(T) = \{3.3mW - 2.4mW + 0.3mW\} + \{3.8mW - 3.1mW + 0.3mW\}$$

$$P_{SCB}(T) = 2.2mW$$

Thus, the total average short-circuit dissipation of the circuit in Figure 4 is:

$$P_{SC}(T) = P_{SCA}(T) + P_{SCB}(T) = 4.4mW$$

The above simulations were carried out for transistor device ratio of $Wp/Wn = 1$. In the case of NAND and NOR gates, Wp and Wn were computed as an effective parallel or series combination. The circuit in Figure 4 was simulated for different Wp/Wn ratios and the results are tabulated in Table 1. The term P_d, average dynamic power, in column four was computed as the difference between $P_{ave}(T)$ and $P_{SC}(T)$. Column five depicts the power efficiency P_{SC}/P_d.

V. Conclusion

A circuit simulation technique for measuring average short-circuit power dissipation in complementary integrated circuits was described. The technique is applicable to circuits which have no current flow during a circuit's steady state operation other than leakage current. The scheme requires a SPICE circuit configuration in which the voltage output state of each cascaded logic stage inverts the incoming voltage state. This technique utilizes power meter pairs to isolate the average short-circuit current from the total average current, thereby providing the average short-circuit power dissipation. Short-circuit power dissipation expressions were derived and simulation results for a differently ratioed Wp/Wn CMOS circuit presented. This technique for simulating average short-circuit power dissipation is most applicable in the design of low power customized circuits and for characterizing the power efficiency of standard cell libraries.

VI. Acknowledgment

The discussions and criticisms of Mr. Eby Friedman, Mr. Richard North and Mr. Kay-Cheng Chew are gratefully acknowledged.

VII. References

[1] S.M. Kang, "Accurate Simulation of Power Dissipation in VLSI Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 5, pp. 889-891, October 1986.

[2] G.J. Fisher, "An Enhanced Power Meter for SPICE2 Circuit Simulation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 7, No. 5, pp. 641-643, May 1988.

[3] H.J. Veendrick, "Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits," *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 4, pp. 468-473, August 1984.

[4] L.W. Nagel, *SPICE2: A Computer Program to Simulate Semiconductor Circuits*, Memo **ERL-M520**, University of California, Berkeley, May 1975.

Table 1
Power dissipation component measurements for Figure 4 as Wp/Wn varies with fixed load, input transition times, and signal Period T.

W_{p/W_n} Ratio	P_{ave}	P_{sc}	P_d	P_{sc/P_d}
	(mW)	(mW)	(mW)	
2/3	16.02	5.93	10.09	0.59
1	13.1	4.4	8.7	0.50
3/2	9.35	2.95	6.3	0.47
2	8.7	2.7	6.0	0.45

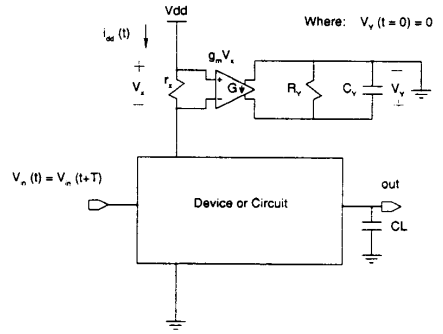

Figure 1. A circuit connected to a voltage-controlled current source and a parallel RC circuit for measuring the average power consumption by directly reading $V_Y(T)$.

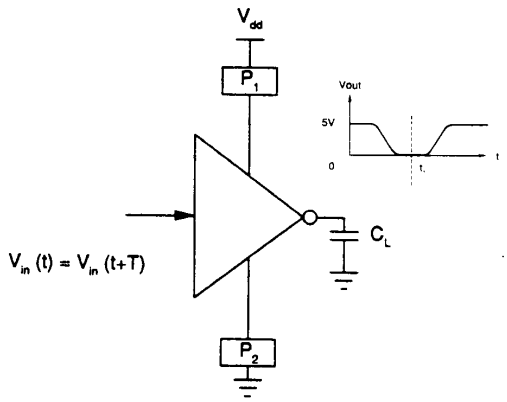

Figure 2. Power meter pair connection across basic CMOS inverting buffer

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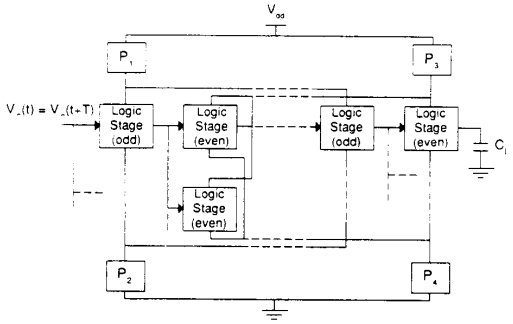

Figure 3. A circuit set-up which permits simulation of average short-circuit power consumption by utilizing the power meter pair concept. The power meter pairs are P_1, P_2 and P_3, P_4.

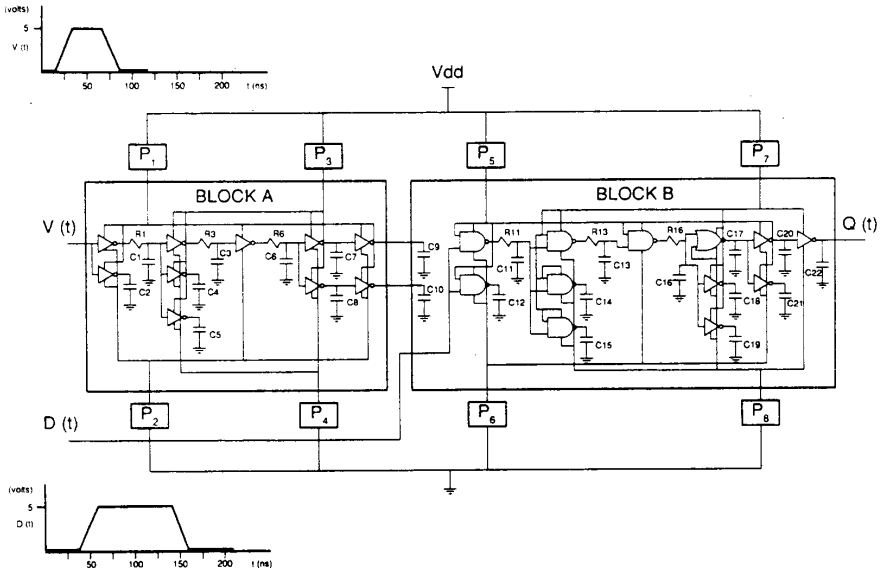

Figure 4. A CMOS circuit, consisting of two sections, used to simulate average short-circuit power consumption. The set-up of each section follows the convention described in part (b) and illustrated in Fig. 2. The combinational readings of the power-meter pairs conveniently supplies the average short-circuit power dissipated during circuit simulation.

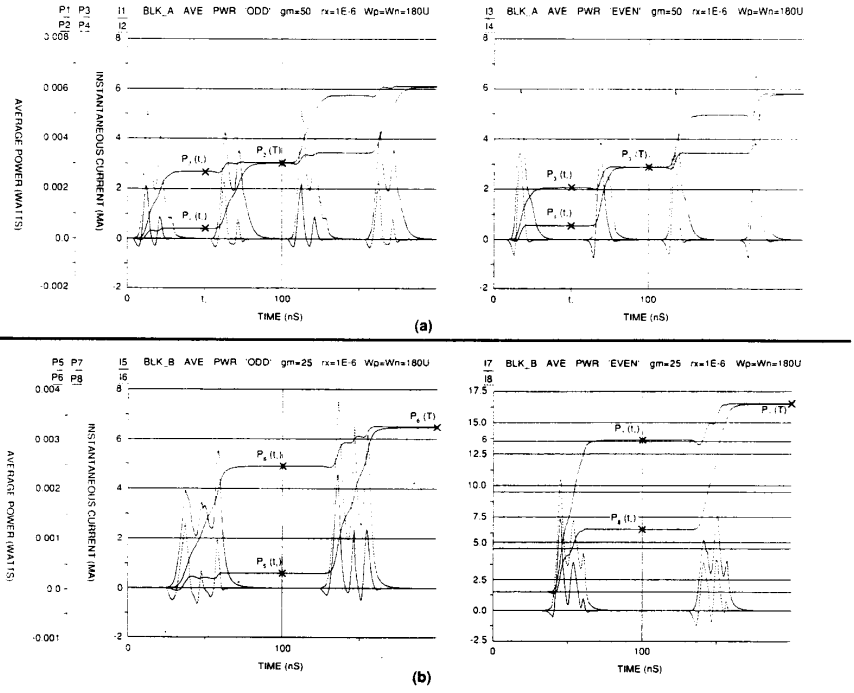

Figure 5. Average short-circuit power consumption SPICE curves for the circuit in Fig. 4. The curves in (a) characterize block A and the curves in (b) charcterize block B.

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Further information can be obtained from **Dr. W. Kenneth Jenkins.**