SLAC-PUB-5518
April 1991
(E/I)

DEVELOPMENT OF PIXEL DETECTORS FOR SSC VERTEX TRACKING*

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ABSTRACT

A description of hybrid PIN diode arrays and a readout architecture for their use as a vertex detector in the SSC environment is presented. Test results obtained with arrays having 256×256 pixels, each 30 μm square, are also presented. The development of a custom readout for the SSC will be discussed, which supports a mechanism for time stamping hit pixels, storing their xy coordinates, and storing the analog information within the pixel. The peripheral logic located on the array, permits the selection of those pixels containing interesting data and their coordinates to be selectively read out. This same logic also resolves ambiguous pixel ghost locations and controls the pixel neighbor read out necessary to achieve high spatial resolution. The thermal design of the vertex tracker and the proposed signal processing architecture will also be discussed.

INTRODUCTION

Pixel detectors are uniquely suited for vertex tracking close to the beam-line in high energy accelerators such as the Superconducting Super Collider. Their unique characteristics are a result of their small sensitive area, which is generally less than 10^4 square microns. The detectors described herein are silicon PIN diode arrays.

* Work supported by Department of Energy contract DE-AC03-76SF00515.

Contributed to the Third Annual International Industrial Symposium on the Super Collider, Atlanta, Georgia, March 13-15, 1991

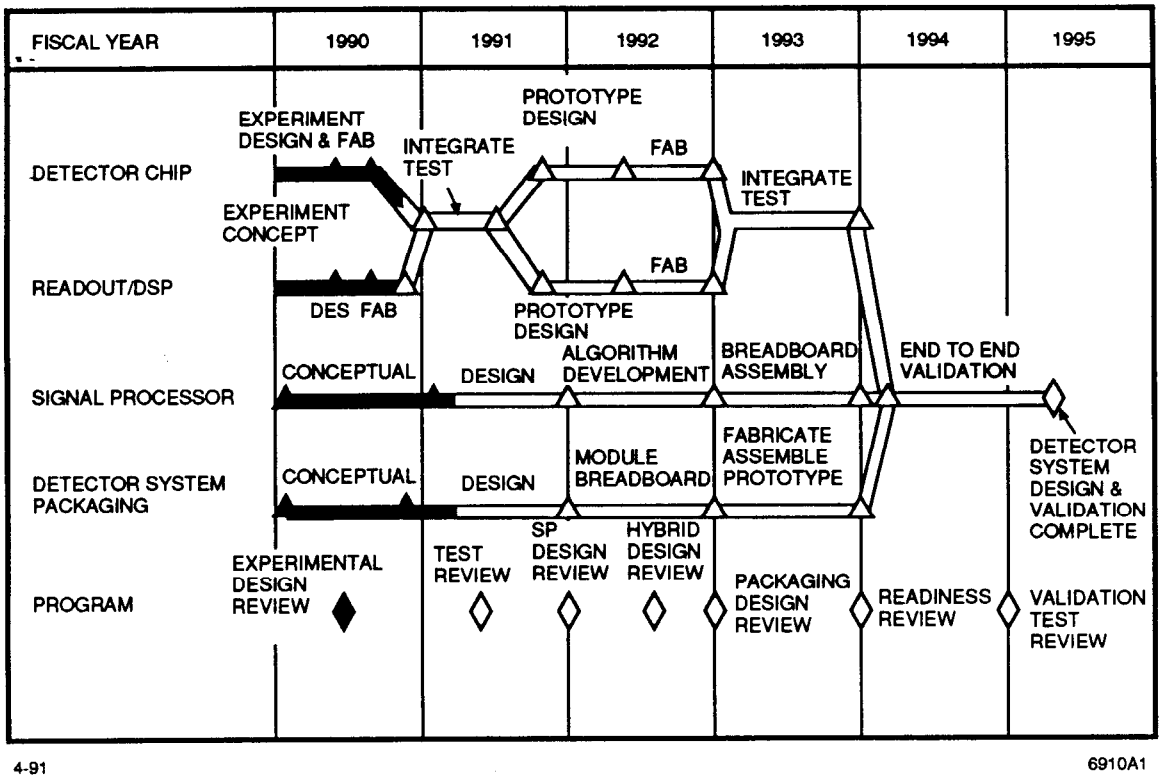

Fig. 1. SSC pixel development time line.

A principal benefit is high resolution position determination to better than 10 μm accuracy. The resulting high resolution tracking provides for accurate momentum measurements and the determination of secondary vertices. Interesting events in the Super Collider will come from the decay of short lived particles which travel a short distance from the primary interaction point and then decay, creating a secondary vertex. Additionally, the pixel's small area allows high track densities and multiple interactions to be resolved, since the probability of multiple hits within the same detector during an event is small. Lastly, the low pixel capacitance results in a signal to noise ratio from minimum ionizing particles of greater than fifty to one. This allows for improvements in system design and a reduction in the effects of radiation. The signal-to-noise ratio degrades due to an increase in noise from radiation induced increases in dark current. The small pixel area results in an exceptionally small initial dark current. Pixel detectors are, thus, well suited to applications close to the beam-line where radiation dosages are highest.

Hughes Aircraft Company is participating in a pixel detector development collaboration with high energy physicists from various universities and national laboratories.[1] This collaboration has been in place for the last two years. Many of the tests and results described in this paper, however, are attributable to the earlier effort funded by the SSC Generic Research Program.[2] The collaboration hopes to capitalize on the technology developed by Hughes Aircraft Company through defense department contracts related to infrared sensor technology over the last 20 to 30 years. The long range plan of the collaboration is the development of a validated end-to-end pixel detector system which can serve as a vertex detector at the SSC. This plan is shown in Fig. 1. The collaboration is presently on schedule, in having demonstrated a working room-temperature hybrid pixel array,[3] and is presently designing and testing the first pixel detectors designed specifically for SSC application.[4] Together with the design of the individual detector chips, the collaboration is pursuing the overall system design. This design includes the detector, the electrical interconnections, the cable packaging, the mechanical and thermal design, and the signal processing. The successful implementation of a vertex detector requires consideration of these system issues in the early stages of development.

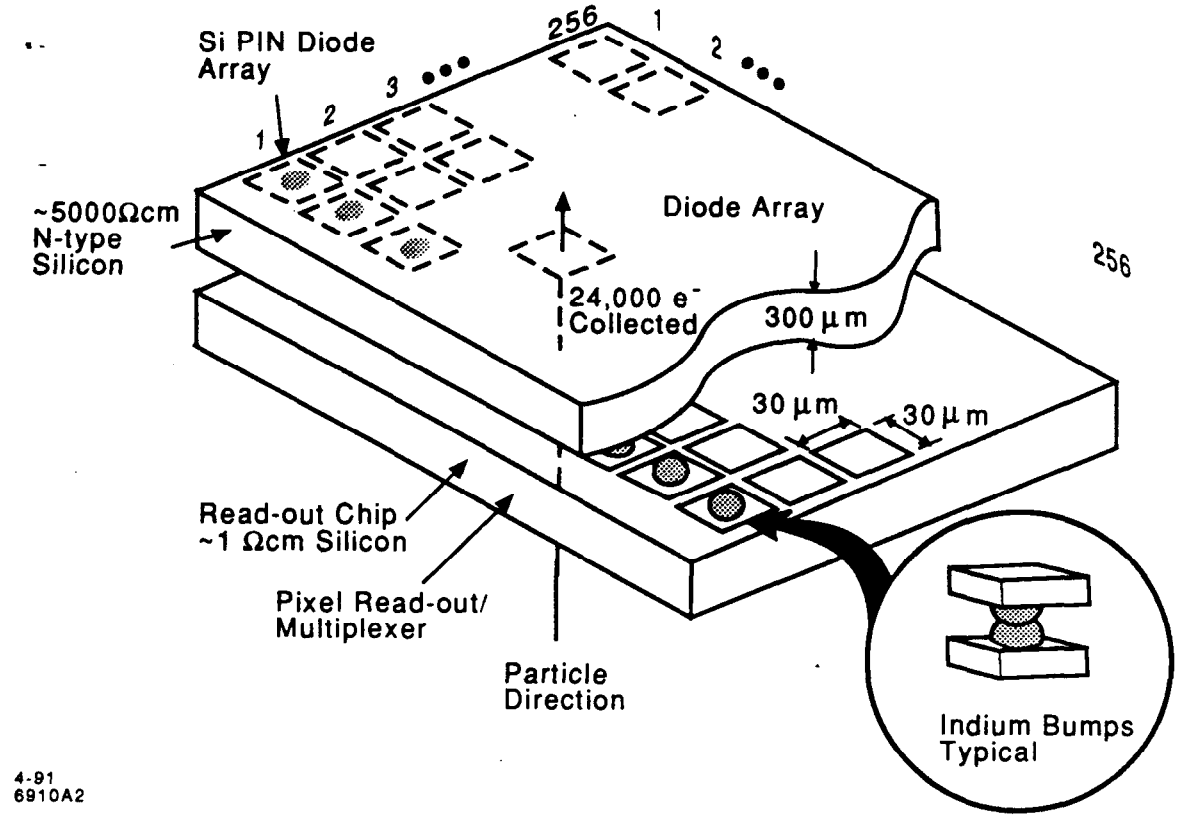

Fig. 2. Schematic Representation of pixel detector hybrid.

PIXEL ARRAYS

The individual detector arrays employ the hybrid approach which has proved extremely successful for infrared sensor arrays. A detector chip, which is an array of silicon PIN diodes, is connected via indium bump interconnects to another silicon array of readout unit cells.

The hybrid approach allows each array to be processed separately and individually optimized. Thus, one can change either the detector design or the readout design more readily. From a manufacturing point of view the yield losses in the detector and readout processing are not compounded because they can each be individually selected prior to hybridization. This is shown schematically in Fig. 2. Figure 3 is a photo of a pixel detector array tested last year. It uses an existing x-y scanned readout. This is a 256 × 256 array with 30 μm square pixels . A detector of this type was exposed to

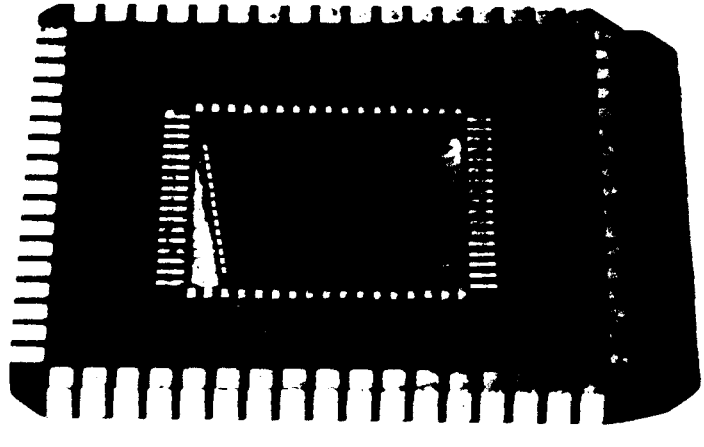

Fig. 3. Photograph of 256 × 256 Array having 30 μm square pixels.

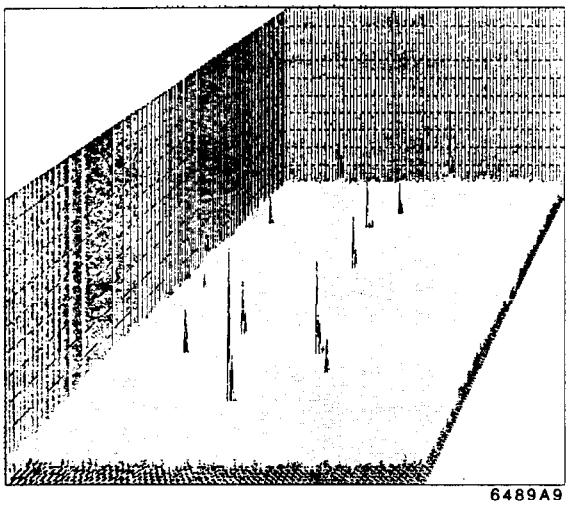

Fig. 4. Plot of 250 GeV/c pions being detected as they traverse a 256×256 array illustrating the strengths of two-dimensional readout to aid in pattern recognition.

250 GeV/c pions at Fermilab, and produced signals with a high signal to noise ratio. A plot of the output of one of these pixel detector arrays is shown in Fig. 4. This plot can be viewed as a proof-of-concept that a significant improvement in pattern recognition can be obtained with two dimensional pixel detectors. Accurate x-y positioning of the particle hit within the 30 μm pixel area is shown. High signal to noise ratios, greater than 50:1 were obtained and charge sharing between adjacent pixels is also evident, thus, allowing very accurate determination of the center of the charge cloud created by the incident particle.

The SSC environment imposes unique requirements on the readout electronics due to its high interaction rate. It is not feasible to read out every pixel in a frame by scanning each frame completely since the beams cross every 16 ns. Therefore, a smart readout is required which allows one to record only those pixels which have been hit. A further level of data reduction is the sparse readout feature, which allows the selection of only those hits deemed interesting by an external trigger. Thus the data rate is significantly reduced by reading out only those pixels which have been hit during interesting events.

Table 1. SSC Prototype Array Parameters

Parameter	Goal
Array format	64×32
Pixel dimension	50 μm $\times$ 150 μm
Time stamp	50 ns
Digital address storage	2 hits/trigger level 1
Smart/sparse readout	Yes
Ghost elimination	Yes
Analog data storage	Yes
Maximum signal	50,000 $e-$
Minimum signal definition	3,000 $e-$
Noise at room temperature	≤ 300 e^-
Power	20 μW/pixel
Readout time	< 10 μs/array

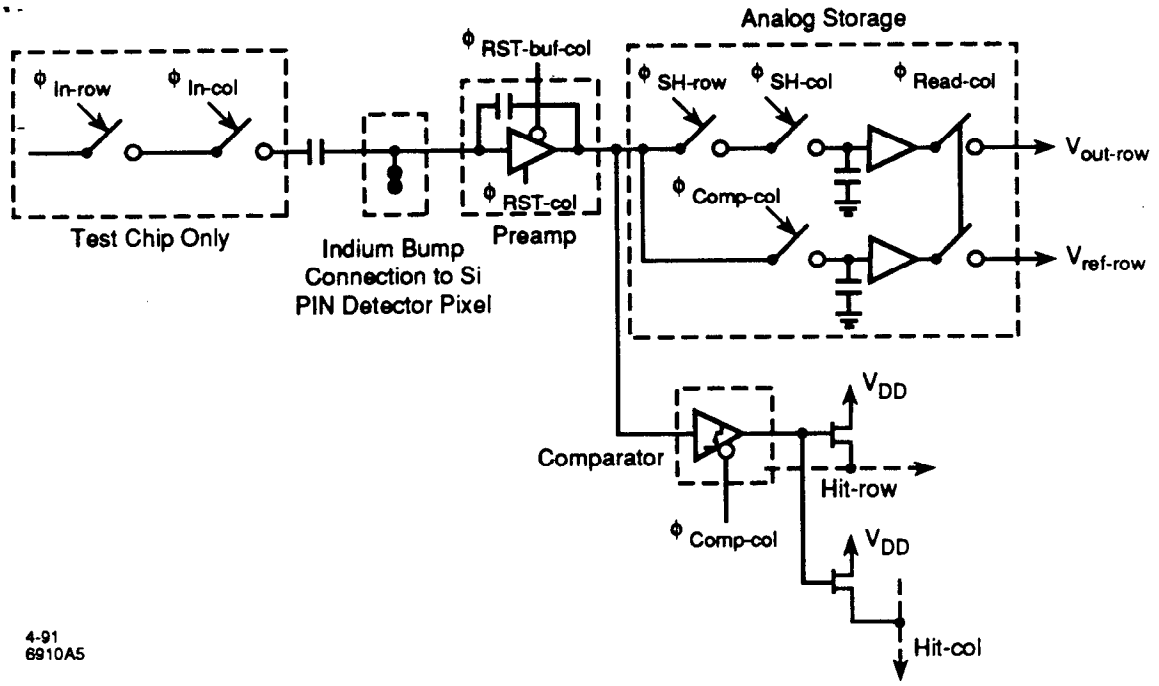

Fig. 5. Schematic of the simplified unit cell architecture.

SSC PROTOTYPE

A readout is under development to meet the SSC requirements. The pixel dimensions are 50 μm × 150 μm in a 64 × 32 array. The goals set for this first prototype are listed in Table 1. The critical parameters are a noise level of less than 300 electrons rms at room temperature, power dissipation of less than 20 μW per pixel, a readout time for the array of less than 10 μs, and the ability to time stamp an event within 50 ns. The unit cell architecture is shown in Fig. 5. The unit cell behind each pixel detector includes an amplifier, analog storage, and an analog comparator. Following a first level trigger, one can return to the pixel and retrieve the stored analog charge within. The test chip, which is a precursor to the prototype array is shown in Fig. 6. This chip allows one to simulate a hit in a pixel by inputting electronically a signal to the unit cell. There is an output signal which indicates that a hit occurred within the array. The hit-row and hit-column signals are read out on serial outputs on the periphery. One can then go back and, using the row and column select lines, read out the analog signal.

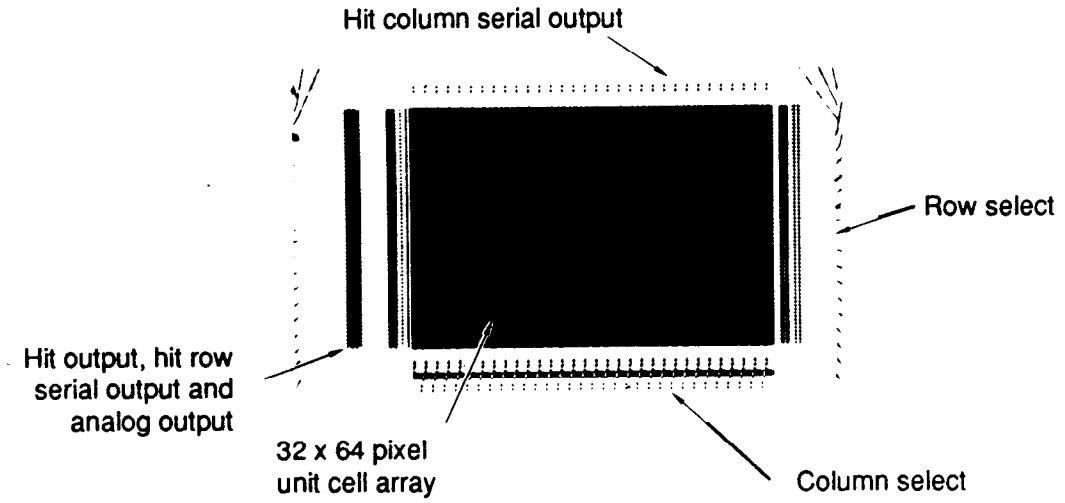

Fig. 6. Photograph of the 32 × 64 SSC array under evaluation.

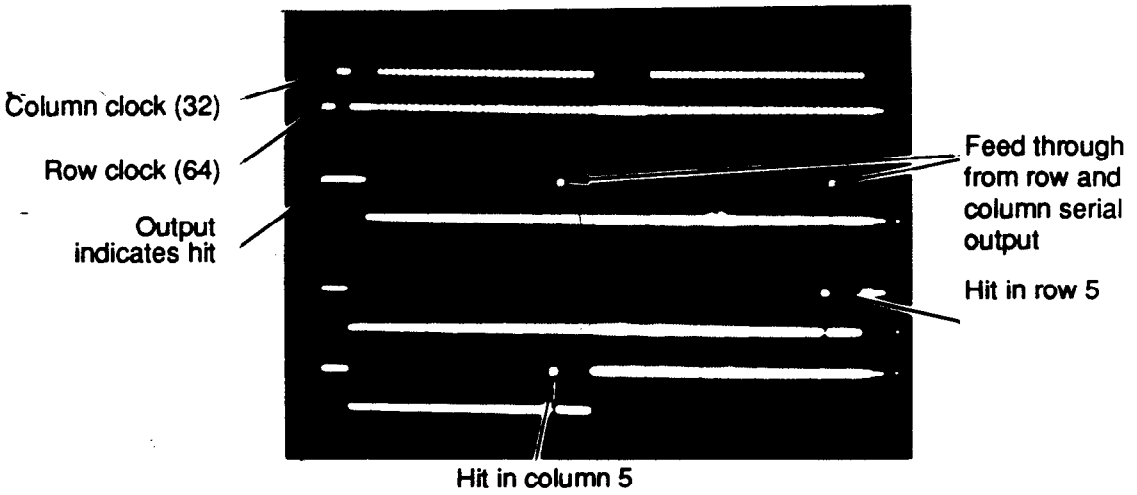

Fig. 7. Scope photograph of the SSC array readout demonstrating the time stamping and the recording of the digital address. Analog information in stored in the pixel for later retrieval.

Figure 7 illustrates the smart readout operation on a test chip. A signal simulating the deposition of a charge of 5,000 electrons is input via the test row and column inputs to the pixel at the intersection of column 5 and row 5. The scope photograph shows the column and row clocks on the upper trace. The scope trigger is at the extreme left of the trace, and the clock duration is set to two microseconds per clock pulse. The second trace is the output hit, which is indicated by the rising edge of the signal. The hit signal and the strobing of the charge into the pixel are simultaneous to within the resolution of this photo. The spurious pulses on this trace represent cross talk within the prototype array, and are generated by the digital signals on the row and column output lines. Their cause has been determined and is being eliminated on the next prototype array. The row and column outputs can be interpreted as a FIFO and locate the row 5 and column 5 position of the hit. Thus, the array indicates a hit on a specific pixel at a specific time. The hit information is stored in memory, and the analog information is stored in the unit cell for later retrieval. Figure 8 is a photograph showing an analog signal being retrieved from the selected pixel, (in this case, a 25000 electron signal in row 3, column 3). The upper trace is the output of the 32 rows (only 22 shown) of column 3 and the output analog signal is seen in row 3. Thus, the test array has demonstrated the smart and sparse readout capability. The second iteration of this array prototype will be hybridized to a detector array for further testing.

RADIATION HARDNESS

The present array is fabricated in a nonradiation hard, L_{eff} equal 1.2 μm, single poly, double metal (pitch = 3.5 μm) CMOS process. Subsequent processing will

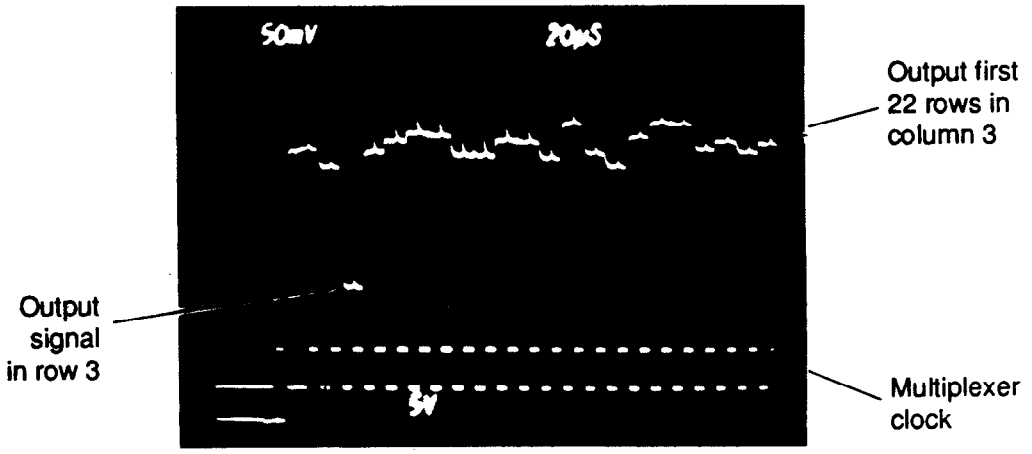

Fig. 8. Scope photograph of the analog readout from a selected pixel.

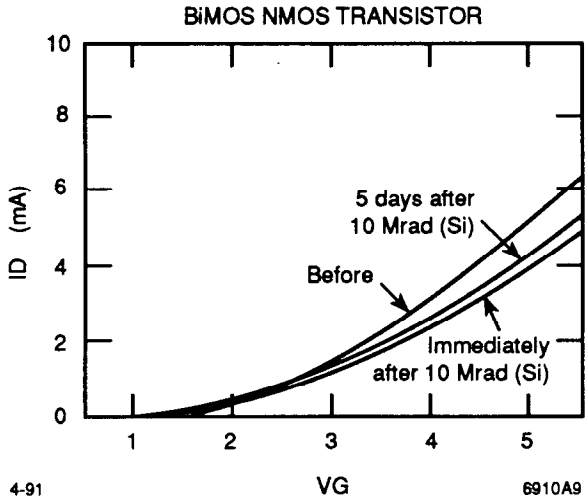

Fig. 9. Curve of drain current versus gate voltage of an NMOS transistor before and after irradiation with 10 MRad of ionizing radiation.

be done using a radiation hard process. An example of a radiation hard process in hand at Hughes Aircraft Company is illustrated in Fig. 9. The transfer characteristics of an NMOS transistor are measured both before and after a 10 MRad dose of ionizing radiation[5] and a 25% drop in drain current observed. To completely demonstrate radiation hardness, the actual circuit under discussion must be irradiated. To this end, the unit cell readout described in this paper has also been fabricated in a radiation hard SOS/CMOS process and a number of die await testing in the laboratory.

THINNED READOUT

In the design of a complete vertex detector system, one must be concerned with its total mass. Silicon detectors previously used in high energy physics have been 300 μm thick. The proposed detector array of PIN diodes discussed in this paper should also be of the order of 300 μm thick for optimal signal-to-noise. Using the hybrid approach, the readout chip, which is also in the path of the particle, will introduce additional mass to the detector array. One might naively view this technology as a doubling of the mass of the system. This, however, is not the case. Figure 10 illustrates the ability to back-thin the readout from its initial thickness of 300 μm to 50 μm after the hybrid has been created and tested. This technique has been used on a number of Hughes projects in the past producing thinned, working arrays. The hybrid pictured here has a 300 μm thick PIN detector and a 50 μm-thick readout for a total of thickness of 350 μm of silicon.

MECHANICAL AND THERMAL DESIGN

Figure 11 shows a proposed mechanical design for the vertex tracker. A significant feature of this design is the use of a ceramic foam of silicon carbide (SiC) as a structural element. The pixel detector arrays are mounted in a louvered fashion on the barrel cylinders and mounted flat on the end cap disks. The SiC foam which has a density of 3% of bulk SiC has a radiation length of 337 cm, and offers a minimal mass for scattering and a porosity which allows gas cooling of the system. A 1-cm thick foam support structure is equivalent in scattering mass to that of a detector hybrid, about 0.3% of a radiation length each. The ability to machine the SiC foam to provide the necessary reference surfaces is shown in Fig. 12. Boron carbide, not used here, is also available as a foam at 3% of its bulk density. This foam has a radiation length of 693 cm, but has slightly worse thermal characteristics. The use of ceramic foams provides a uniform mass distribution design with minimal frame structure thereby reducing mass concentrations. The gas cooling system adds no contribution to the scattering mass, and requires no assembly or maintenance. Table 2 summarizes the benefits of this unique design.

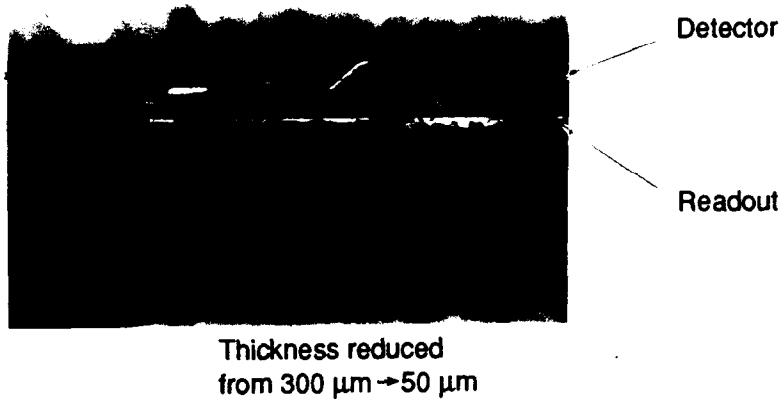

Fig. 10. Photograph of a working detector hybrid which has been back-thinned so that the readout electronics is only 50 μm thick.

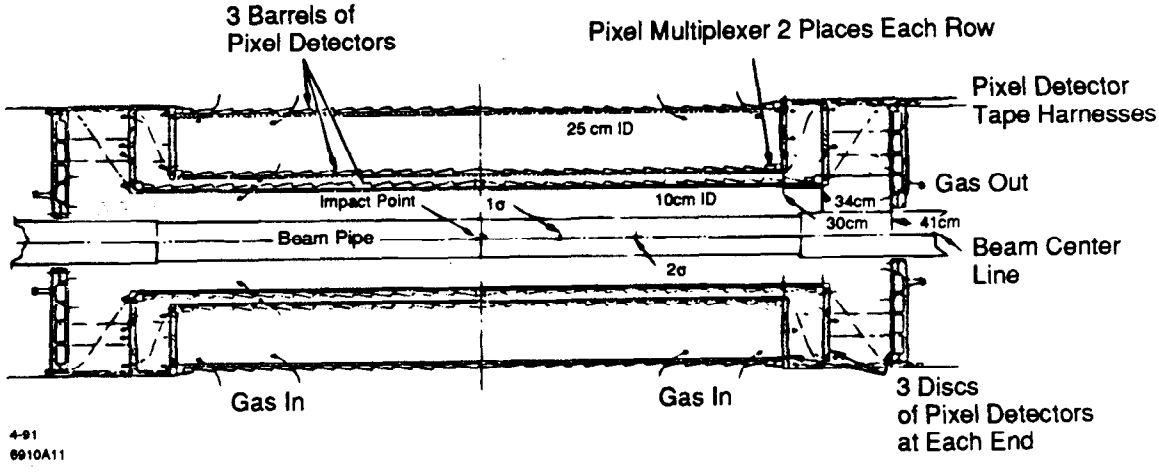

Fig. 11. Schematic representation of the proposed mechanical design of a three layer vertex detector for the SSC, showing the silicon carbide (SiC) foam structural features, including the gas cooling.

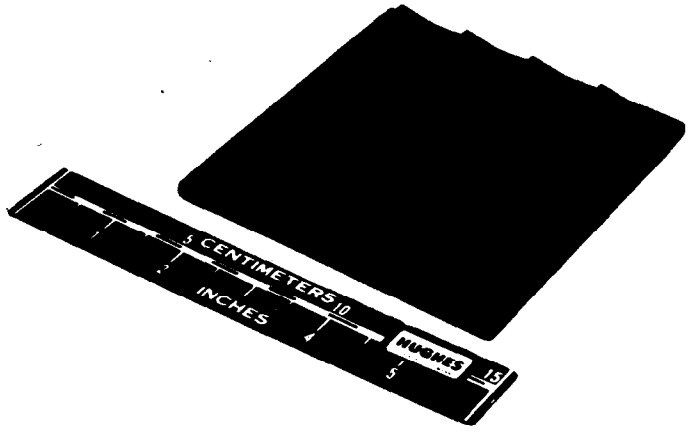

Fig. 12. Photograph of a SiC foam substrate demonstrating its machineability.

Table 2. Features of the Present Design Concept Related to the Design Requirements

REQUIREMENT / FEATURES	MINIMUM RADIATION LENGTH	THERMAL DISSIPATION	POSITIONAL ACCURACY	EASE OF ASSEMBLY MAINTENANCE	COVERAGE η =0–2.5 (90° – 10° COVERAGE)	RADIATION HARDNESS	LONG LIFE
STRUCTURE OF CERAMIC FOAM MONOCOQUE	TOTAL MASS <10% RADIATION LENGTH UNIFORM DISTRIBUTION	-COMBINED HEAT TRANSFER & STRUCTURAL FUNCTION	RESOLUTION <10 μm R, θ	-REPEATABLE MACHINING & ASSEMBLY	-OVERLAPPED CHIPS FOR ~100% FILL FACTOR	>10 Mrads	>10 YEARS
GAS COOLING	NEGLIGBLE CONTRIBUTION	-33°C TO 0°C OPERATING RANGE 0.25 W/cm^2 (average)	-RESOLUTION <25 μm in Z DIRECTION	-NO ASSEMBLY -NO MAINTENANCE	-NO CONCENTRATED MASS	-UNAFFECTED	>>>10 YEARS
MODULAR DESIGN 1 PIXEL CHIP 9 STRIP CHIPS 144 SUBASSYS			-LARGE SUBASSYS REDUCES TOLERANCE BUILDUP	-REMOVABLE SUBASSY -VERTEX DET. REMOVABLE FOR TRACKER CALIBRATION	-FULL COVERAGE ACHIEVED		MODULES CAN BE REPLACED

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Laboratory tests have shown that passing nitrogen gas through SiC foam at velocities of about 40 cm/s can dissipate 0.25W/cm^2 with a temperature differential of about 4°C across one layer.

The mechanical design uses one basic pixel detector array which is 2 cm × 2 cm, and the complete system of barrels and end caps contains 3,004 chips. The louvered construction provides and overlapping of chips for a 100% lapping fill factor. If one were to retain the pixel size at 50 μm ×150 μm, and orient the 150 μm dimension along the beam axis, then one would achieve a spatial resolution of about 10 μm rms in the azimuthal direction, and about 30 μm rms in the z direction. It is anticipated that in the final design, the long dimension can be reduced. Should we elect to do so, the spatial resolution in the z direction will be reduced as well.

SIGNAL PROCESSING

To complete the system design, one needs to consider the system architecture. The concept presently being explored uses an intermediate data acquisition chip to collect the signals from up to 64 pixel arrays for data compression and sequencing. The multiplexed data is then sent to an outside demultiplexer and momentum and vertex processor to determine the track parameters. The decision to send data from the pixel arrays to the data acquisition chip is made by a first level trigger which comes from sources external to the vertex detector, generally from a calorimeter. In some experiments, parameters from the pixel data could be used as part of the first level trigger. The signal processing architecture is shown in Fig. 13. Table 3 is referred to as an N^2 chart. Various hardware elements of the system are shown on the diagonal. The columns contain the inputs to each of the hardware element, and the rows contain the outputs of each hardware element. Thus, for the data acquisition chip, one can see the inputs coming from the pixel detector hit data, and command inputs from the controller. The outputs from that chip would be a bit stream going out to the smart demultiplexer, sequence commands, to the pixel detectors, and status information to the controller.

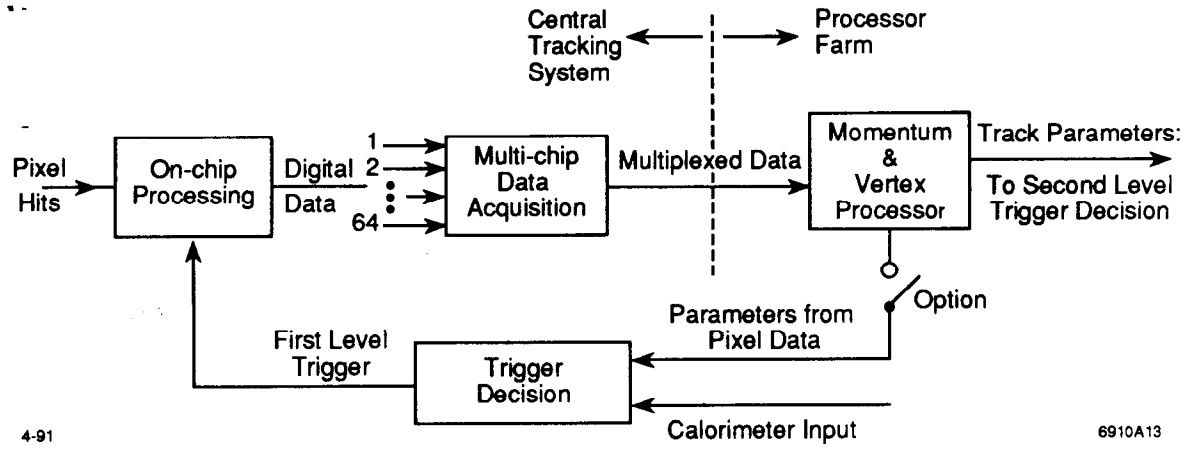
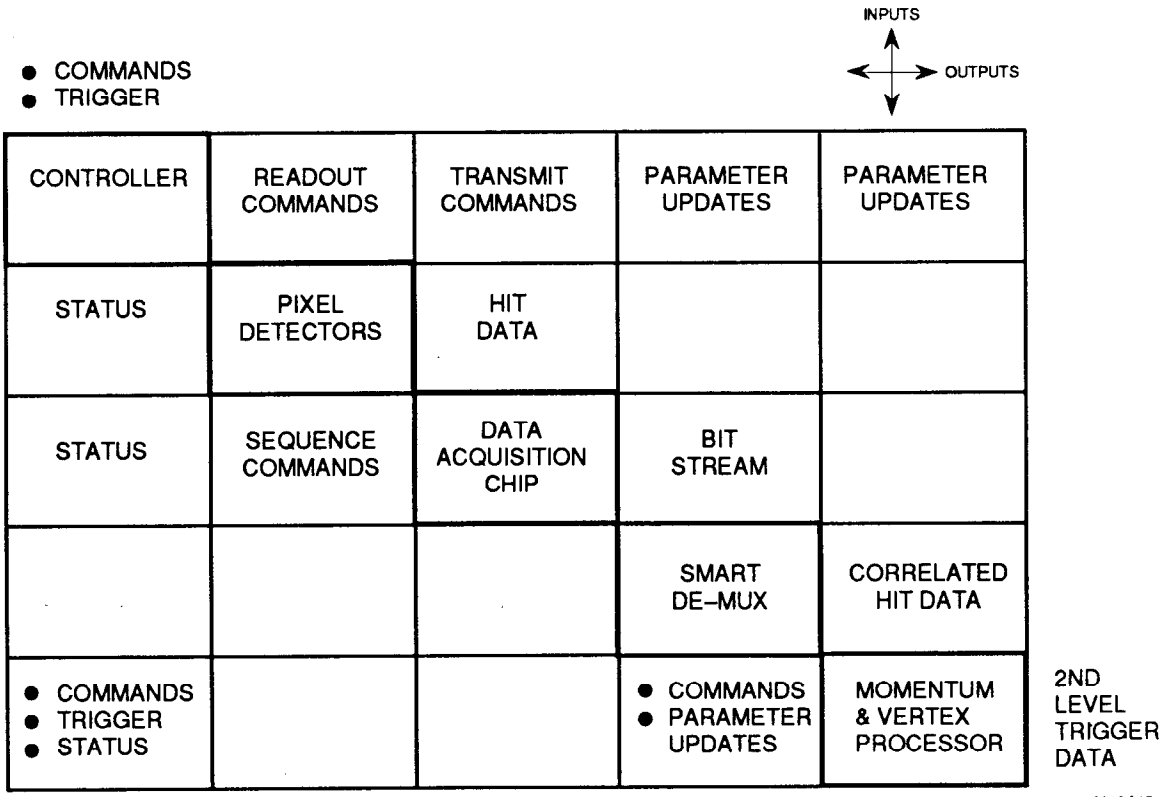


Fig. 13. Schematic representation of a strawman pixel signal and data processor architecture.

SUMMARY

Development is proceeding on schedule for the design of a complete pixel detector subsystem. A proof of principle demonstrating the advantages of room-temperature, hybrid, two-dimensional pixel detectors has been achieved. Similarly, a preprototype array has demonstrated the smart, sparse readout concept under development. Radiation hard processing is available for implementation of the readout electronics. A mechanical and thermal design concept has been established which is a simple low mass, modular, design. The ability to produce thinned hybrids has been demonstrated, and signal processing and architecture issues are being addressed.

Table 3. An N^2 Chart for the Pixel Signal and Data Processor



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